# MX·COM, INC.

# MX709

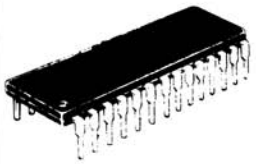
## Voice Store Retrieve CVSD Codec

### FEATURES:

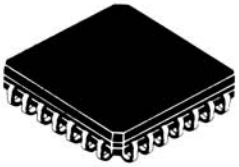
- **Delta Modulation Encoding**
- **Bytewide Storage and Control**
- **Programmable Sampling Rate and Filter**
- **Low Power CMOS Requirements**
- **Microprocessor-Friendly**

### APPLICATIONS:

- **Digital Speech Communications**
- **Digital Scrambling**
- **Voice Message Mailbox**
- **Speech Analysis**
- **Voice Multiplexing**
- **Speech Compression**



**MX709J (CDIP)**
**MX709P (PDIP)**
**28 pins**



**MX709LH8**
**(28p PLCC)**

### DESCRIPTION:

The MX709 is a continuously variable slope delta modulation (CVSD) codec for a wide variety of digital audio processing applications. Its primary use is in microprocessor-controlled voice storage and retrieval systems.

In the encode mode, audio input signals are band-limited by a lowpass filter and digitized by a CVSD 1-bit serial encoder. After conversion to 8-bit parallel format, encoded data is read to the data bus for storage in memory.

In the decode mode, memory contents written into the data bus are converted back to 1-bit serial form and decoded by a CVSD decoder. The decoder output is lowpass filtered and output as retrieved audio.

The audio encode/decode functions are independently controlled, permitting concurrent or asynchronous VSR operations. Time and frequency companding is available via independently programmable encode/decode data rates and filter cut-offs.

Support of VOX functions and "Pause" memory management is provided by the power assessment register. This register contains two 4-bit numbers representing the average signal levels into the data encoder and a replica encoder over a programmable averaging period.

The device instruction set includes input/output signal switching and a standby power-save function. The MX709 is a low power CMOS circuit and requires only a single 5V supply.



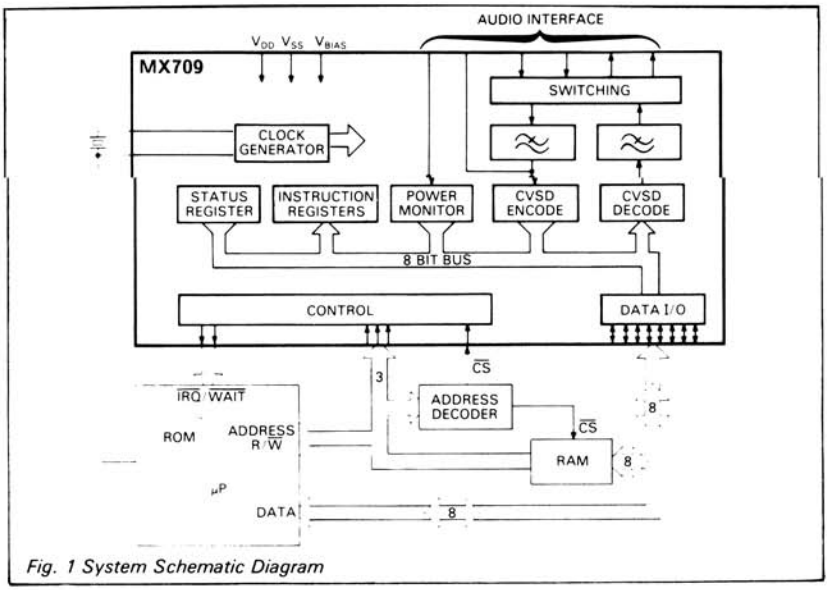



*Fig. 1 System Schematic Diagram*

# MX709 PIN FUNCTION TABLE

| PIN | FUNCTION/DESCRIPTION |
|---|---|

**MX709J, P**
**MX709LH**

**1** **$\overline{\text{Xtal/Clock}}$:** Output of a clock oscillator inverter.

**2** $A_0$
**3** $A_1$ ┐ These pins determine which register may be addressed via the I/O Port.
**4** $R/\overline{W}$ ┘

Table

| $A_0$ | $A_1$ | $R/\overline{W}$ | Register |
|---|---|---|---|
| 0 | 0 | 0 | 'A' instruction |
| 1 | 0 | 0 | 'B' instruction |
| 0 | 1 | 0 | Decoder |
| 1 | 1 | 0 | No register |
| 0 | 0 | 1 | Status |
| 1 | 0 | 1 | Power |
| 0 | 1 | 1 | Encoder |
| 1 | 1 | 1 | No register |

**5** **$\overline{\text{CS}}$:** Chip select input, this input has 1MΩ pullup to $V_{DD}$.

**6** $D_0$ ┐
**7** $D_1$ │
**8** $D_2$ │
**9** $D_3$ ├ **I/O port**
**10** $D_4$ │
**11** $D_5$ │
**12** $D_6$ │
**13** $D_7$ ┘

**14** **$\overline{\text{IRQ}}$:** Interrupt request output (100KΩ pullup), this pin is the output of the interrupt request generator. This device can be "wire OR'd" with other active low components. See section on Interrupt Requests.

**15** **No Connection**

**16** **No Connection**

**17** **Analog output B:** *(See Fig. 4.)*

**18** **Analog output A:** *(See Fig. 4.)*

**19** **$V_{Bias}$:** This is the bias or analog ground pin and is internally set to $V_{DD}/2$. It should be decoupled to $V_S$ with a capacitor of 1.0μF (min.).

**20** **Analog input A:** *(See Fig. 2, Note 4 and Fig.4)*

**21** **$V_{DD}$:** Positive supply.

**22** **Analog input B:** *(See Fig. 2, Note 4 and Fig. 4)*

**23** **No Connection.**

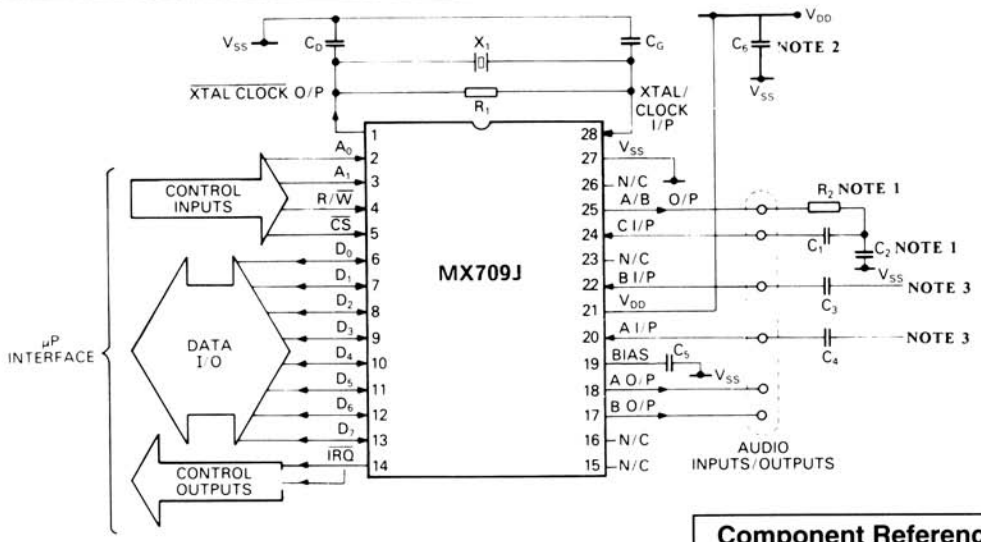
**24** **Analog input C:** This is the analog input to the power encoder.

**25** **Analog output A/B:** *(See Fig. 4.)*

**26** **No Connection.**

## MX709 PIN FUNCTION TABLE

| PIN | FUNCTION/DESCRIPTION |
|---|---|
| **MX709J, P**<br>**MX709LH** | |
| 27 | **$V_{SS}$:** Negative supply. |
| 28 | **Xtal/Clock Input:** This is the input to the clock oscillator inverter. 1MHz Xtal input or externally derived clock is injected at this pin. |




NOTES:

1. $R_2$, $C_2$ forms a lowpass filter input to "C" input power assessment circuit. The values shown represent a 820 Hz lowpass although other cutoff frequencies may be selected depending on the application.
2. Additional decoupling may be necessary for noisy supplies.
3. To prevent unwanted internal oscillations at the Encoder Input pins, the source impedance to these inputs must be less than 1 Kohm. Ideally, the source impedance should be less than 50 ohms to minimize granular noise.

**Component References**

| Component | Value | Tolerance |
|---|---|---|
| $R_1$ | >1M | ±10% |
| $R_2$ | 5.6k | ±10% |
| $C_G$ | 68p | |
| $C_D$ | 33p | |
| $C_1$ | 0.1μ | ±20% |
| $C_2$ | .033p | ±20% |
| $C_3$ | 0.1μ | ±20% |
| $C_4$ | 0.1μ | ±20% |
| $C_5$ | 1.0μ min. | ±20% |
| $C_6$ | 0.1μ | ±20% |

FIG. 2: EXTERNAL COMPONENT CONNECTIONS

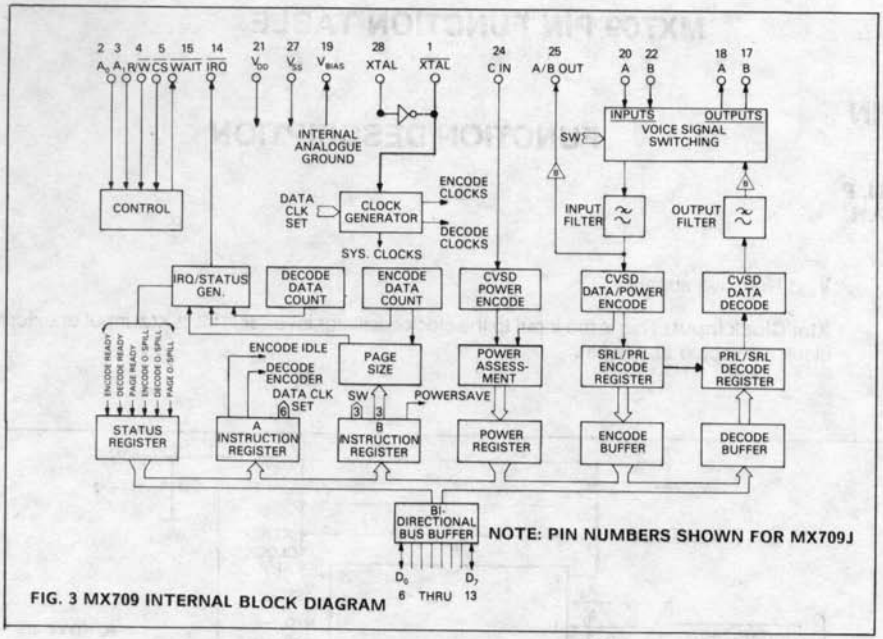
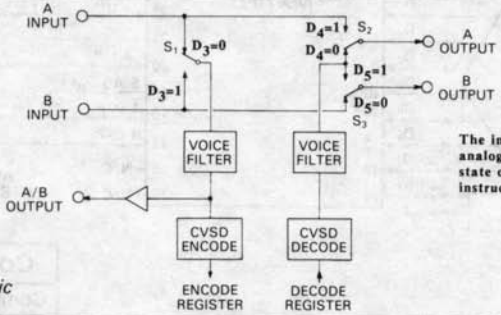



FIG. 3 MX709 INTERNAL BLOCK DIAGRAM

## ANALOG SWITCHING




The input and output switching of analog signals is controlled by the state of bits $D_3$, $D_4$, and $D_5$ in instruction register B.

*Fig. 4 Audio Switching — Simplified Block Schematic*

### Frequency and Data Rate Control

Six bits of Instruction Register A **($D_2$-$D_7$)** control the data rates of the encoder and decoder and the bandwidths of the filters for the encoder and decoder. The configuration of the frequency dividers is as shown in the diagrams below and obtainable combinations of frequencies with various input clocks are listed.

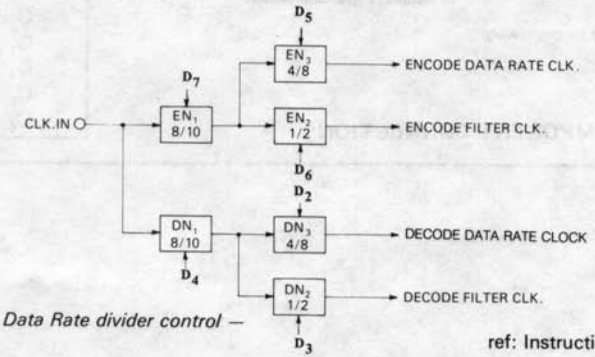



*Fig. 5 Filter Clock and Data Rate divider control — Block diagram*

ref: Instruction Register 'A'

| Clock Input | Encoder Clock Programming Bits in Register A | Decoder Clock Programming Bits in Register A | Filter Clock (Hz) | Lowpass Filter BW pb. ±1dB | Data Clock (kbs) |
|---|---|---|---|---|---|
| 2MHz | 010xxxxx | xxx010xx | 125k | 3320 | 62.5 |
| " | 011xxxxx | xxx011xx | 125k | 3320 | 31.25 |
| " | 110xxxxx | xxx110xx | 100k | 2656 | 50.0 |
| " | 111xxxxx | xxx111xx | 100k | 2656 | 25.0 |
| 1MHz | 000xxxxx | xxx000xx | 125k | 3320 | 31.25 |
| " | 001xxxxx | xxx001xx | 125k | 3320 | 15.625 |
| " | 010xxxxx | xxx010xx | 62.5k | 1660 | 31.25* |
| " | 011xxxxx | xxx011xx | 62.5k | 1660 | 15.625* |
| " | 100xxxxx | xxx100xx | 100k | 2656 | 25.0 |
| " | 101xxxxx | xxx101xx | 100k | 2656 | 12.5 |
| " | 110xxxxx | xxx110xx | 50k | 1328 | 25.0* |
| " | 111xxxxx | xxx111xx | 50k | 1328 | 12.5* |
| 2.048MHz | 010xxxxx | xxx010xx | 128k | 3400 | 64.0 |
| " | 011xxxxx | xxx011xx | 128k | 3400 | 32.0 |
| " | 110xxxxx | xxx110xx | 102.4k | 2720 | 51.2 |
| " | 111xxxxx | xxx111xx | 102.4k | 2720 | 25.6 |
| 1.024MHz | 000xxxxx | xxx000xx | 128k | 3400 | 32.0 |
| " | 001xxxxx | xxx001xx | 128k | 3400 | 16.0 |
| " | 010xxxxx | xxx010xx | 64k | 1700 | 32.0* |
| " | 011xxxxx | xxx011xx | 64k | 1700 | 16.0* |
| " | 100xxxxx | xxx100xx | 102.4k | 2720 | 25.6 |
| " | 101xxxxx | xxx101xx | 102.4k | 2720 | 12.6 |
| " | 110xxxxx | xxx110xx | 51.2k | 1360 | 25.6* |
| " | 111xxxxx | xxx111xx | 51.2k | 1360 | 12.6* |
| 614.4kHz | 001xxxxx | xxx001xx | 76.8k | 2040 | 9.6* |
| 768.0kHz | 101xxxxx | xxx101xx | 76.8k | 2040 | 9.6* |

*Table 1 Possible combinations of clock input frequency, filter cutoff (Hz) and Data Clock (kbs)*

**Caution: Although possible, the Codec insertion loss is not according to the specification at these settings.*

## Register Truth Tables

The following tables describe the function of each bit within each register. 'Address Input' logic states are shown in the top right hand corner of each table. The following registers are described below:

Instruction Register 'A' [IRA]
Instruction Register 'B' [IRB]
Status Register [SR]
Power Register [PR]

**IRA** **INSTRUCTION REGISTER 'A'**

$A_0 = 0$
$A_1 = 0$
$R/\overline{W} = 0$

| Bit | Function Name | Logic State | References | NOTES |
|---|---|---|---|---|
| $D_0$ | Encoder Idle | | $SRD_3$ | $D_0$ sets the encoder idle/normal mode of operation. |
| | | 1 | | **FORCED:** Forces the encode register to fill with a 1010101... idle pattern. *Note: incoming encoded data is still available for the power assessment circuits.* |
| | | 0 | | **NORMAL:** Allows the encode register to fill with encoded data. Data is transferred to the encode buffer during the last bit of the encode byte. |
| $D_1$ | Decoder Data Source | | $SRD_4$ | $D_1$ determines the source of data for the decoder. |
| | | 1 | | **ENCODER:** Internally connects the output of the encode register to the input of the decode register. This condition effectively connects the audio straight through. The encoded data may still be accessed via the encode buffer, and data bus. |
| | | 0 | | Fills the decoder register with idle pattern. In either case data may be loaded into the decoder register via the data bus. This automatically overwrites the current contents of the decoder register. |
| $D_2$ | Decode Data Rate Clock Divider | | Fig. 5 Table 1 | $D_2$ sets the Decode data rate divider. |
| | | 1 | | ÷ 8 |
| | | 0 | | ÷ 4 |
| $D_3$ | Decode Filter Clock Divider | | Fig. 5 Table 1 | $D_3$ sets the Decode Filter Clock Divider and hence the Filter Cut-off Frequency. |
| | | 1 | | ÷ 2 |
| | | 0 | | ÷ 1 |
| $D_4$ | Decode Master Clock Divider | | Fig. 5 Table 1 | $D_4$ sets the Decode Master clock divider. |
| | | 1 | | ÷ 10 |
| | | 0 | | ÷ 8 |

## IRA — INSTRUCTION REGISTER 'A'

$A_0 = 0$
$A_1 = 0$
$R/\overline{W} = 0$

| Bit | Function Name | Logic State | References | NOTES |
|---|---|---|---|---|
| $D_5$ | Encode Clock Divider | 1 | Table 1 | $D_5$ sets the Encode Data Rate Divider. ÷ 8 |
| | | 0 | | ÷ 4 |
| $D_6$ | Encode Filter Clock Divider | 1 | Table 1 | $D_6$ sets the Encode Filter Clock Divider and hence the filter cut-off frequency. ÷ 2 |
| | | 0 | | ÷ 1 |
| $D_7$ | Encode Master Clock Divider | 1 | Table 1 | $D_7$ sets the Encode Master Clock Divider ÷ 10 |
| | | 0 | | ÷ 8 |

## IRB — INSTRUCTION REGISTER 'B'

$A_0 = 1$
$A_1 = 0$
$R/\overline{W} = 0$

| Bit | Function Name | Logic State | References | NOTES |
|---|---|---|---|---|
| $D_0$ | Page Size Set | | | $D_0$-$D_2$ set the "page size" in Encode Data bytes. (one byte = 8 serial data bits) in accordance with the table below: |
| $D_1$ | | | | |
| $D_2$ | | | | |

| $D_2$ | $D_1$ | $D_0$ | : | PAGE BYTES | Page period @ 32 kbs |
|---|---|---|---|---|---|
| 0 | 0 | 0 | : | 32 | 8ms |
| 0 | 0 | 1 | : | 64 | 16ms |
| 0 | 1 | 0 | : | 96 | 24ms |
| 0 | 1 | 1 | : | 128 | 32ms |
| 1 | 0 | 0 | : | 160 | 40ms |
| 1 | 0 | 1 | : | 192 | 48ms |
| 1 | 1 | 0 | : | 224 | 56ms |
| 1 | 1 | 1 | : | 256 | 64ms |

Page Period (sec) = 8 × Page Bytes/Data Rate (b/s)

| | | | | |
|---|---|---|---|---|
| $D_3$ | "A/B" Encode | | Fig. 4 | $D_3$ defines which audio input A or B is connected to the encoder via the encode filter. (See fig. 4). |
| | | 0 | | **AUDIO INPUT "A":** Internally connects the "A" audio input to the encode filter input. The "A/B OUT" pin outputs filtered audio "A." Audio input "B" set to $V_{DD}/2$. |
| | | 1 | | **AUDIO INPUT "B":** Internally connects the "B" audio input to the encode filter input. The "A/B OUT" pin controls filtered audio "B." Audio input "A" set to $V_{DD}/2$. |

**IRB** **INSTRUCTION REGISTER 'B'**

$A_0 = 1$
$A_1 = 0$
$R/\overline{W} = 0$

| Bit | Function Name | Logic State | References | NOTES |
|---|---|---|---|---|
| $D_4$ | Switch Audio Output | | Fig. 4 | $D_4$ controls the Output Audio Switch to determine which source audio is connected to Audio Output "A" pin. |
| | "A" | 1 | | Input "A" to Output "A" (direct). |
| | | 0 | | Decoder to Output "A." |
| $D_5$ | Switch Audio Output | | Fig. 4 | $D_5$ controls the Output Audio Switch to determine which source audio is connected to Audio Output "B" pin. |
| | "B" | 1 | | Decoder to Output "B." |
| | | 0 | | Input "B" to Output "B" (direct). |
| $D_6$ | Powersave | | | $D_6$ controls the enablement and disablement of all analog circuit elements. |
| | | 1 | | **POWERSAVE MODE:** Disables the circuit elements, thereby effectively reducing current consumption. |
| | | 0 | | **OPERATING MODE:** All circuit elements enabled. |
| | | | | **NOTE:** During POWERSAVE, inputs are biased $V_{DD}/2$. Outputs are biased $V_{DD}/2$ if IRB $D_4/D_5$ are set to "direct." |
| $D_7$ | Power Sensitivity | | | $D_7$ determines the sensitivity range of the power measuring circuits. |
| | | 1 | | **HIGH:** Low power input, assessment circuits have + 12dB gain over LOW Setting. |
| | | 0 | | **LOW:** Normal power assessment sensitivity range. |
| | | | | **NOTE:** High input levels in the HIGH condition may lead to overflow, producing an ambiguous reading. |

## SR — STATUS REGISTER

$A_0 = 0$
$A_1 = 0$
$R/\overline{W} = 1$

| Bit | Function Name | Logic State | References | NOTES |
|---|---|---|---|---|
| $D_0$ | Encode Data Ready | | | $D_0$ indicates that a byte of data has been encoded and can be read from the encode buffer. |
| | | 1 | | **READ BYTE:** Set high during the last bit of the byte shifted into the encode register. This condition causes an interrupt request. |
| | | 0 | | **NOT READY/OVERSPILL:** This condition occurs when:<br>1. The last data byte in the encode data register has been read.<br>2.Encode data overspill bit = 1<br>i.e. $SRD_3 = 1$. |
| $D_1$ | Decode Data Ready | | | $D_1$ indicates that a byte of data has been decoded and a new byte should be written to the decode buffer. |
| | | 1 | $SRD_4$ | **WRITE BYTE:** This condition occurs when the decode register has been loaded from its buffer, i.e. after the last bit of the previous byte has been clocked out of the register. |
| | | 0 | | **NOT READY/OVERSPILL:** This condition occurs when data has been written into the decode buffer or the decode data overspill condition is valid (**$SRD_4 = 1$**). |
| $D_2$ | Page Ready | | | This bit indicates that a page of bytes has been encoded. |
| | | 1 | | **READ PAGE:** This condition occurs when the page counter has completed the last byte of a page. This is after power measurements have been written into $PRD_0$ to $PRD_7$ inclusive. |
| | | 0 | $SRD_5$ | **NOT READY/OVERSPILL:** This condition occurs when Power Register "PR" has been read or the page overspill condition is valid. |
| $D_3$ | Encode Overspill | 1 | | **OVERSPILL:** Indicates that the encode data was not read between two consecutive "encode data ready" flags. Encoded data bytes have been lost, and no further bytes will be transferred to the encode buffer. |
| | | 0 | | **NORMAL:** This condition occurs when data has been read from the encode buffer, following a data ready flag, $SRD_0 = 1$, or by writing to the decode buffer if both encode and decode overspill bits are set. |

## SR — STATUS REGISTER

$A_0 = 0$
$A_1 = 0$
$R/\overline{W} = 1$

| Bit | Function Name | Logic State | References | NOTES |
|---|---|---|---|---|
| $D_4$ | Decode Overspill | 1 | | **OVERSPILL:** When this bit is set data transfer from the decode buffer to the decode register is inhibited. If the "DECODER/ENCODER BUS" **($IRAD_1$)** is not set then the decode register will fill with idle pattern. |
| | | 0 | | **NORMAL:** This condition occurs when data has been written to the decode buffer following a data ready flag, $SRD_1 = 1$, or by reading the contents of the encode buffer if both encode and decode overspill bits are set. |
| $D_5$ | Page Overspill | 1 | | **OVERSPILL:** This state indicates that the power register was not read before the next page was completed. |
| | | 0 | | **NORMAL:** Power register "read" or IRB written. |

## PR — POWER REGISTER

$A_0 = 1$
$A_1 = 0$
$R/\overline{W} = 1$

| Bit | Function Name | Logic State | NOTES |
|---|---|---|---|
| $D_0$ | "A/B" Power LSB | | $D_0$-$D_3$ represent the average signal level of the last page of data in the range from + 6dBm to - 24dBm (at 1kHz) for the A or B input. (0dBm = 775mVRMS) |
| $D_1$ | | | The relationship between binary value and signal level is frequency dependent and exhibits pre-emphasis characteristics. (see fig. 8.) |
| $D_2$ | | | |
| $D_3$ | "A/B" Power MSB | | |
| $D_4$ | "C" Power LSB | | |
| $D_5$ | | | $D_4$-$D_7$ represent the average signal level of the last page of data in the range from + 6dBm to - 24dBm (at 1kHz) for the C input. |
| $D_6$ | | | |
| $D_7$ | "C" Power MSB | | |

## Interrupts

Three conditions can cause interrupt requests to the host microprocessor.
(i) The encoder buffer contains an unread byte of data which is the most recent byte encoded.
(ii) The decode buffer is ready to receive the next consecutive byte for decoding.
(iii) The power register contains a power assessment for the most recent whole page encoded.

The status register indicates which of the above conditions are true.

If an interrupt condition remains unserviced and the condition becomes irrecoverably untrue, the status bit is cleared, the corresponding overspill bit is set, and further interrupts are automatically inhibited. Also the encode and decode data buffers retain the data present when the data bit was set, i.e. register-buffer update is inhibited. The power register is updated at all times.

Condition (i) is serviced by a valid address to the encode buffer. Condition (ii) is serviced by a valid address to the decode buffer. If conditions (i) and (ii) have both become UNTRUE, servicing either buffer resets both to a clear start position. Condition (iii) is serviced by reading the Power Register.

## The C Input

By careful selection of the audio frequency filtering to the C input, the A/B and C power words can be used in the processor to provide frequency as well as power information. This facility could be used for word, pause or voice recognition.

# MX709 ELECTRICAL SPECIFICATIONS

## Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

| | | |
|---|---|---|
| Supply voltage | | −0.3V to 7.0V |
| Input voltage at any pin (ref. $V_{ss}$ = OV) | | −0.3V to ($V_{DD}$ + 0.3V) |
| Output sink/source current (total) | | 20mA |
| Operating temperature range: | MX709J | −30°C to + 85°C |
| | MX709LH,P | −30°C to + 70°C |
| Storage temperature range: | MX709J | −55°C to + 125°C |
| | MX709LH,P | −40°C to + 85°C |

## Operating Limits

All characteristics measured using the following parameters unless otherwise specified: $V_{DD}$ = 5V, $T_{amb}$ = 25°C, ∅ = $f_{in}$ = 1MHz

| Characteristics | See Note | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Static Characteristics** | | | | | |
| Supply Voltage | | 4.5 | 5.0 | 5.5 | V |
| Supply Current | | — | 6 | — | mA |
| Supply Current (Power Save) | | — | 1 | — | mA |
| Supply Ripple | | — | 50 | — | mV |
| Input Impedance (Audio) | | 100 | — | — | kΩ |
| Output Impedance (Audio) | | — | — | 6 | kΩ |
| Input Logic '1' | | 3.5 | — | — | V |
| Input Logic '0' | | — | — | 1.5 | V |
| Output Logic '1' | 1 | 3.5 | — | — | V |

# MX709 ELECTRICAL SPECIFICATIONS (cont.)

| Characteristics | | See Note | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static Characteristics (cont.)** | | | | | | |
| Output Logic '0' | | 1 | — | — | 1.5 | V |
| Input Current (Logic I/P's) | | | — | — | 1.0 | µA |
| Input Capacitance (Logic I/P's) | | | — | — | 7.5 | pF |
| Output Logic '1' Source current | | 2 | — | — | 120 | µA |
| Output Logic '0' Sink current | | 3 | — | — | 360 | µA |
| Three State output leakage current | | | — | — | 4 | µA |
| **Dynamic Characteristics** | | | | | | |
| Audio Input Level | | | — | 500 | — | mV (rms) |
| Insertion Loss (Direct) | | 4, 7 | -1.5 | — | +1.5 | dB |
| Attenuation distortion (See fig. 6) | | | | | | |
| Clock bit Rate | | 5 | 8 | — | 64 | k bits/sec |
| Idle Channel Noise | | 4, 6 | — | 2.5 | — | mV (rms) |
| Signal/Noise Ratio (see fig. 8) | | | | | | |
| **Timing Information** | | | | | | |
| Address Set up time | (tAS) | 8 | 50 | — | — | ns |
| Read Write Set up time | (tRWS) | 8 | 50 | — | — | ns |
| Address Hold time | (tAH) | 8 | 0 | — | — | ns |
| Read Write Recovery time | (tRWR) | 8 | 0 | — | — | ns |
| Chip Select Access time | (tACS) | 8 | — | — | 250 | ns |
| Output Hold time (read) | (tOHR) | 8 | 0 | — | 100 | ns |
| Data Set up time (write) | (tDSW) | 8 | 150 | — | — | ns |
| Data Hold time (write) | (tDHW) | 8 | 50 | — | — | ns |

**Notes**

1. *Load 50pF, 200kΩ*
2. *$V_{out}$ = 4.6V, not pins 12 ($\overline{IRQ}$) and 15 ($\overline{Wait}$), these pins have 100kΩ pullups to VDD.*
3. *$V_{out}$ = 0.4V*
4. *Measured from Codec audio input to audio output.*
5. *2.048MHz master clock ÷ 32*
6. *32kHz clock.*
7. *For a load of > 100kΩ, serial switch impedance is 3kΩ/switch (See Fig. 4).*
8. *See Figure 7 Timing Diagram*

## Typical Performance

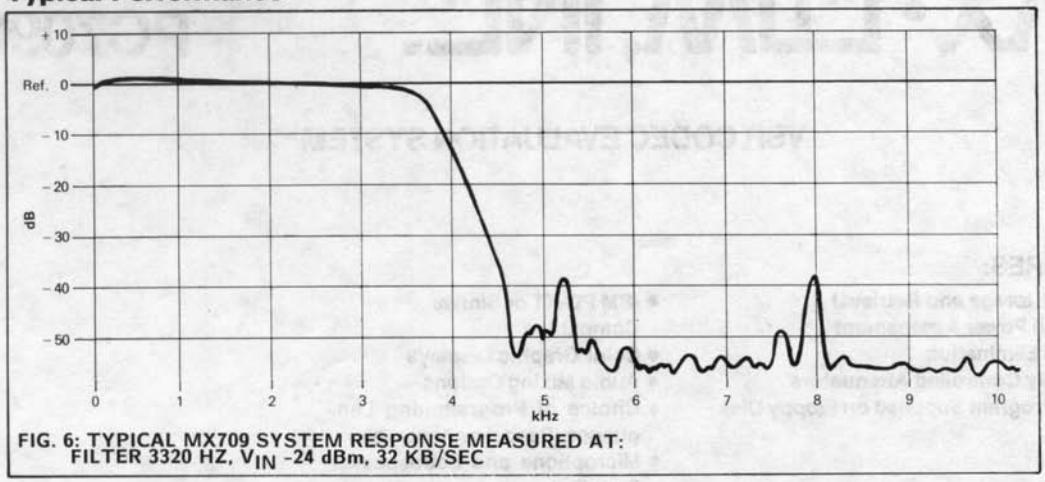
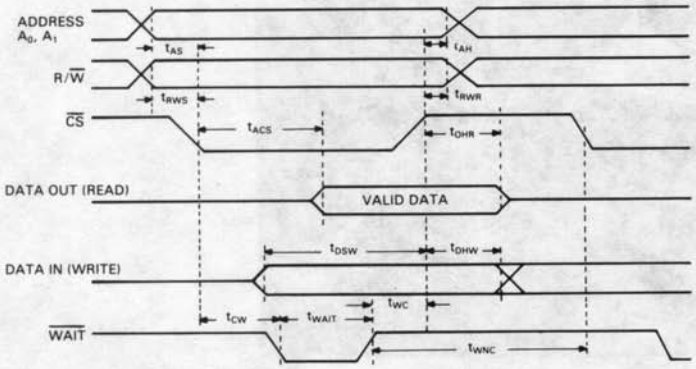



FIG. 6: TYPICAL MX709 SYSTEM RESPONSE MEASURED AT: FILTER 3320 HZ, $V_{IN}$ -24 dBm, 32 KB/SEC




| t= | Min. | Typ. | Max. | Units |
|---|---|---|---|---|
| $t_{AS}$ | 50 | – | – | ns |
| $t_{RWS}$ | 50 | – | – | ns |
| $t_{AH}$ | 0 | – | – | ns |
| $t_{RWR}$ | 0 | – | – | ns |
| $t_{ACS}$ | – | – | 250 | ns |
| $t_{OHR}$ | 0 | – | 100 | ns |
| $t_{DSW}$ | 150 | – | – | ns |
| $t_{DHW}$ | 50 | – | – | ns |
| $t_{CW}$ | – | – | 100 | ns |
| $t_{WAIT}$ | 2 | – | 3 | Xtal Cycle |
| $t_{WC}$ | 0 | – | – | ns |
| $t_{WNC}$ | 2 | – | – | Xtal Cycle |

**KEY**

$t_{AS}$ – Address Set Up Time
$t_{RWS}$ – Read/Write Set Up Time
$t_{AH}$ – Address Hold Time
$t_{RWR}$ – Read/Write Recovery Time
$t_{ACS}$ – Chip Select Access Time
$t_{OHR}$ – Output Hold Time (Read)
$t_{DSW}$ – Data Set Up Time (Write)
$t_{DHW}$ – Data Hold Time (Write)
$t_{CW}$ – Chip Select to WAIT Output
$t_{WAIT}$ – WAIT Time
$t_{WC}$ – WAIT High to Chip Select High
$t_{WNC}$ – End of Wait to Next Chip Select

*Fig. 7 Timing Diagram*

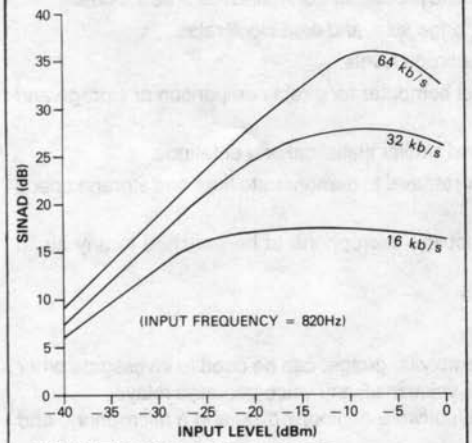



FIG. 8: TYPICAL MX709 SINAD VERSUS INPUT LEVEL

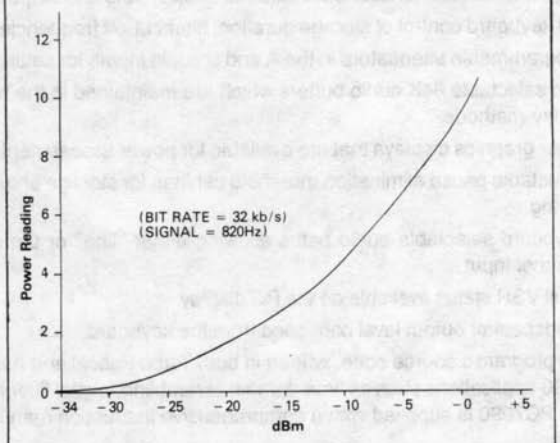



FIG. 9: POWER READING VS. INPUT LEVEL

6

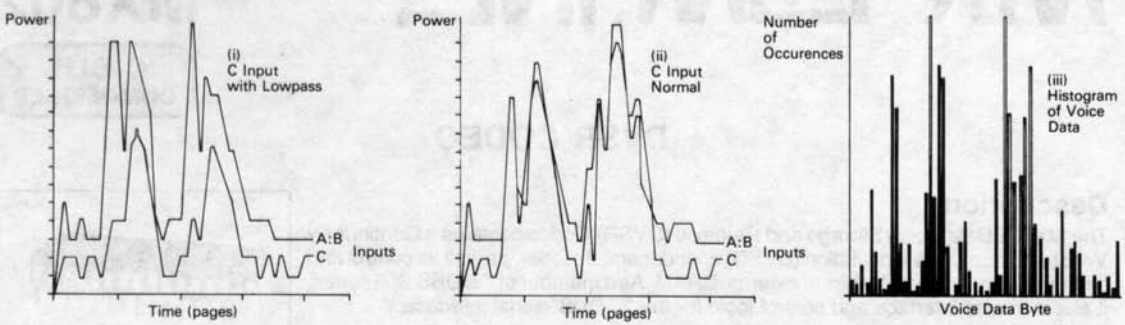



*Fig. 2 Typical Graphical Displays Available*

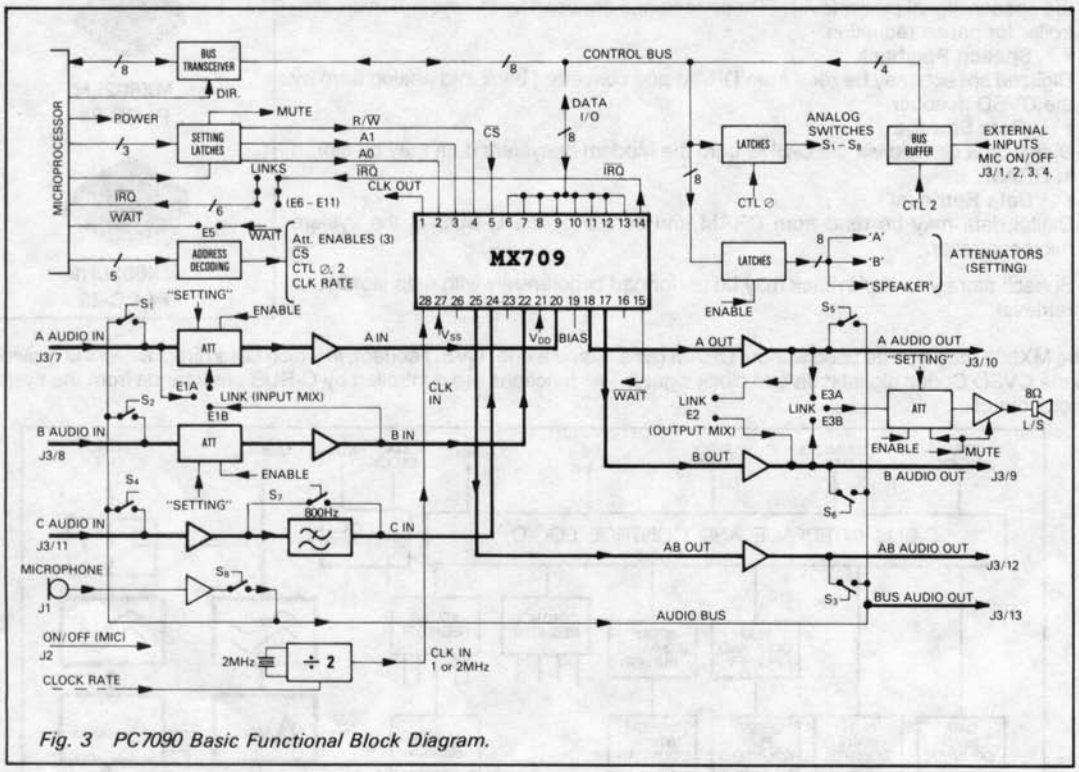



*Fig. 3 PC7090 Basic Functional Block Diagram.*

## ORDERING INFORMATION

**PC7090 EVKIT**

**comprises:** **Plug-in printed circuit board.**
**Program on floppy disk.**
**Instruction manual.**
**Loudspeaker.**
**Microphone.**

*Physical dimensions PCB 13.4 in. × 3.94 in.*